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(54) A microcontroller accessible macrocell

(57) A circuit connectable to a microcontroller having an address bus, a data bus, a read line and a write line including a programmable logic device (PLD) array, at least one input pin and at least one databus macrocell. The input pin is connected to the PLD array and is connectable to the address bus. The databus macrocell is connected to the PLD array and to an external unit and is also connectable to the data bus, the read line and the write line. The data bus directly accesses the databus macrocell.

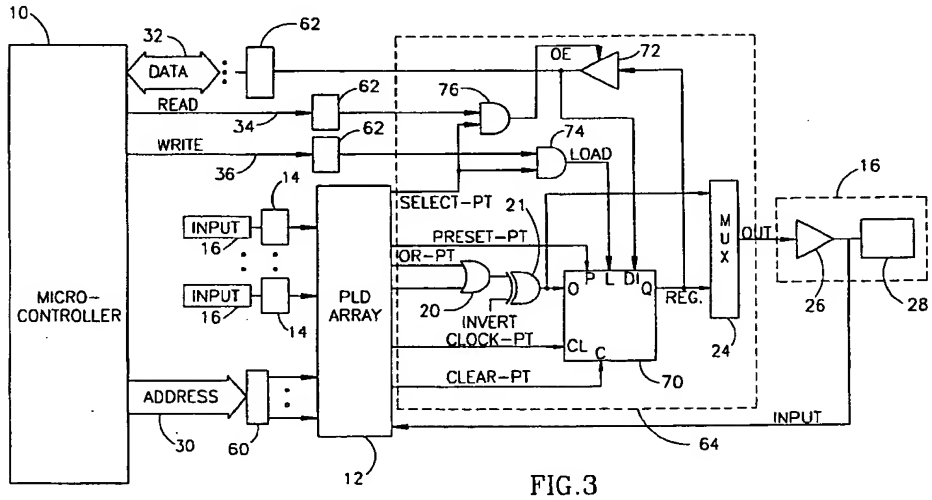

FIG.3

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address information through PLD array 12 additionally requires that the bus signals follow standard timing. Fig. 2, to which reference is now briefly made, illustrates the timing of a single read/write cycle. The microcontroller begins by driving the address bus with an address 50, as indicated in graph A. The address is decoded, usually by an external unit (not shown) and a select signal is generated to the selected peripheral, such as PLD 12. The peripheral then waits for the next phase of the bus cycle when microcontroller asserts either the read or the write signal, as indicated in graph B.

In a read cycle, the peripheral responds by driving the data bus with the required information, labeled 52, and microcontroller 10 latches the data at a rising edge 54 of the read signal. In a write cycle, microcontroller provides data 52 and the peripheral latches data 52 at the rising edge 54 of the write pulse.

It will be appreciated that race conditions can occur between the data and the read/write signals due to violations of the bus setup and hold timing which occur since PLD 12 has delays therein. Furthermore, since the PLD 12 powers up every time it receives a signal, the fact that the address and data busses are connected to the PLD 12 will cause every change in the bus to trigger a power up/power down cycle of PLD 12. This continual cycling adds to power consumption.

Still further, routing the address and data bus data through the macrocells utilizes the critical PRESET, CLEAR, CLOCK and OR product terms, making it hard to implement the remaining logic functions which the PLD array must perform, not to mention the time required to develop the logic functions which respond to the address and data bus signals.

SUMMARY OF THE PRESENT INVENTION

Applicants have realized that, for bus operations to and from the macrocells, there is no need to pass signals from the accessed macrocell through the programmable logic device (PLD). Instead, the data bus and read/write signals can be directly connected to the accessed macrocells and the address bus can be directly connected to the PLD array.

There is therefore provided, in accordance with a preferred embodiment of the present invention, a PLD based circuit connectable to a microcontroller which has an address bus, a data bus, a read line and a write line. The circuit includes the PLD array, at least one input pin connected to the PLD array and connectable to the address bus and at least one databus macrocell. The databus macrocell is connected to the PLD array and to an external unit and is connectable to the data bus, the read line and the write line. The databus macrocell can be directly accessed by the data bus.

There is also provided, in accordance with a preferred embodiment of the present invention, a PLD based circuit connectable to a microcontroller which has an address bus, a data bus, a read line and a write line. The circuit includes the PLD array, at least one input pin connected to the PLD array and connectable to the address bus and at least one databus macrocell. The databus macrocell is connected to the PLD array and to an external unit and is connectable to the data bus, the read line and the write line. The databus macrocell can be directly accessed by the data bus. The databus macrocell includes a data-in flip-flop having at least one data-in input port and an output port for storing a data bit within it, an output buffer connected to the output port of the data-in flip-flop, a data line connectable to the data bus and connected to the data-in input port and the output buffer and read means and write means. The read means are connected to a select line active when the databus macrocell is addressed by the microcontroller and connected to the read line for activating the output buffer to provide the data bit to the data bus. The write means are connected to the select line and the write line for activating the data-in flip-flop to store a data bit provided on the data bus.

There is also further provided, in accordance with a further preferred embodiment of the present invention, a PLD based circuit connectable to a microcontroller. The circuit includes the PLD array, at least one input pin connected directly to the PLD array and connectable to the address bus, at least one macrocell connected to the PLD array with its corresponding input/output pin and at least one databus macrocell. The databus macrocell is connected to the PLD array and has one input/output pin, two input pins and one output pin associated therewith. The input/output pin is connectable to said data bus, the input pins are connectable to the read and write lines and the output pin is connected to the external world.

Additionally, in accordance with a preferred embodiment of the present invention, the databus macrocell includes a data-in flip-flop, an output buffer, a data line, a read unit and a write unit. The data-in flip-flop has at least a data-in input port and an output port for storing a data bit therein. The output buffer is connected to the output port of the data-in flip-flop. The data line is connectable to the data bus and is connected to the data-in input port and the output buffer. The read unit is connected to a select line active when the databus macrocell is addressed by the microcontroller and is connected to the read line. The read unit activates the output buffer to provide the data bit to the data bus. The write unit is connected to the select line and the write line and activates the data-in flip-flop to store a data bit provided on the data bus.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood and appreciated more fully from the following detailed description taken in conjunction with the drawings in which:

claims which follow:

Claims

1. A circuit connectable to a microcontroller having an address bus, a data bus, a read line and a write line, the circuit comprising:

   a programmable logic device (PLD) array;

   at least one input pin connected to said PLD array and connectable to said address bus; and

   at least one databus macrocell, connected to said PLD array and to an external unit and connectable to said data bus, said read line and said write line, which said data bus can directly access.

2. A circuit according to claim 1 and wherein said databus macrocell comprises:

   a data-in flip-flop having at least a data-in input port and an output port for storing a data bit therein;

   an output buffer connected to said output port of said data-in flip-flop;

   a data line connectable to said data bus and connected to said data-in input port and to said output buffer;

   read means connected to a select line active when said databus macrocell is addressed by said microcontroller and connected to said read line for activating said output buffer to provide said data bit to said data bus; and

   write means connected to said select line and said write line for activating said data-in flip-flop to store a data bit provided on said data bus.

3. A databus macrocell connectable to a PLD array and to a data bus, the macrocell comprising:

   a data-in flip-flop having at least a data-in input port and an output port for storing a data bit therein;

   an output buffer connected to said output port of said data-in flip-flop;

   a data line connectable to said data bus and connected to said data-in input port and to said output buffer;

   read means connected to a select line of said PLD array and connected to a read line for activating said output buffer to provide said data bit to said data bus; and

   write means connected to said select line and a write line for activating said data-in flip-flop to store a data bit provided on said data bus.

4. A circuit connectable to a microcontroller having an address bus, a data bus, a read line and a write line, the circuit comprising:

   a programmable logic device (PLD) array;

   at least one input pin connected directly to said PLD array and connectable to said address bus;

   at least one macrocell connected to said PLD array which has one input/output pin associated therewith; and

   at least one databus macrocell connected to said PLD array which has one input/output pin, two input pins and one output pin associated therewith, wherein:

   said input/output pin is connectable to said data bus;

   said input pins are connectable to said read line and said write line; and

   said output pin is connectable to the external world.

5. A circuit according to claim 4 and wherein said databus macrocell comprises:

   a data-in flip-flop having at least a data-in input port and an output port for storing a data bit therein;

   an output buffer connected to said output port of said data-in flip-flop;

   a data line connectable to said data bus and connected to said data-in input port and to said output buffer;

   read means connected to a select line active when said databus macrocell is addressed by said microcontroller and connected to said read line for activating said output buffer to provide said data bit to said data bus; and

   write means connected to said select line and said write line for activating said data-in flip-flop to store

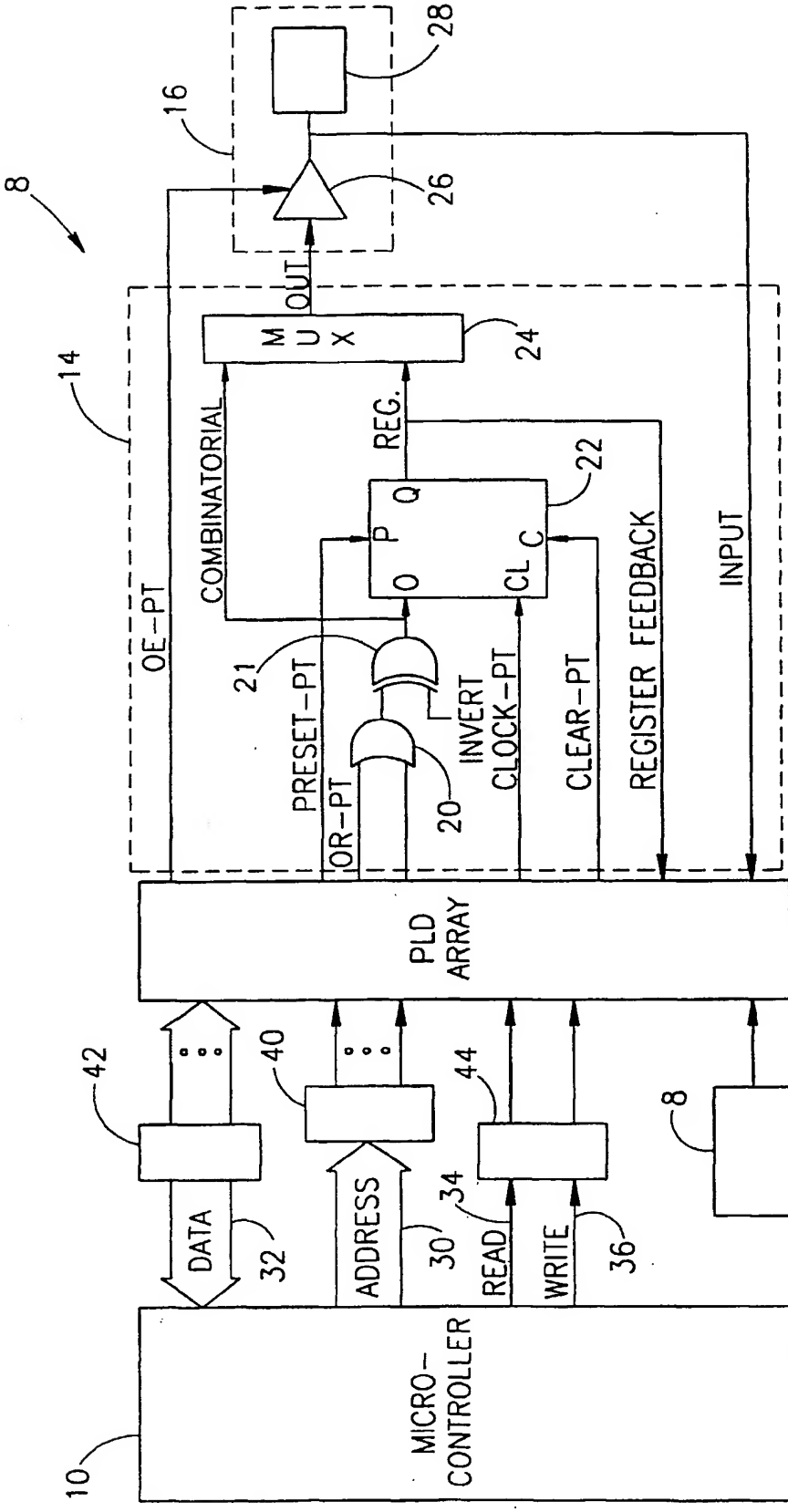

FIG.1
PRIOR ART

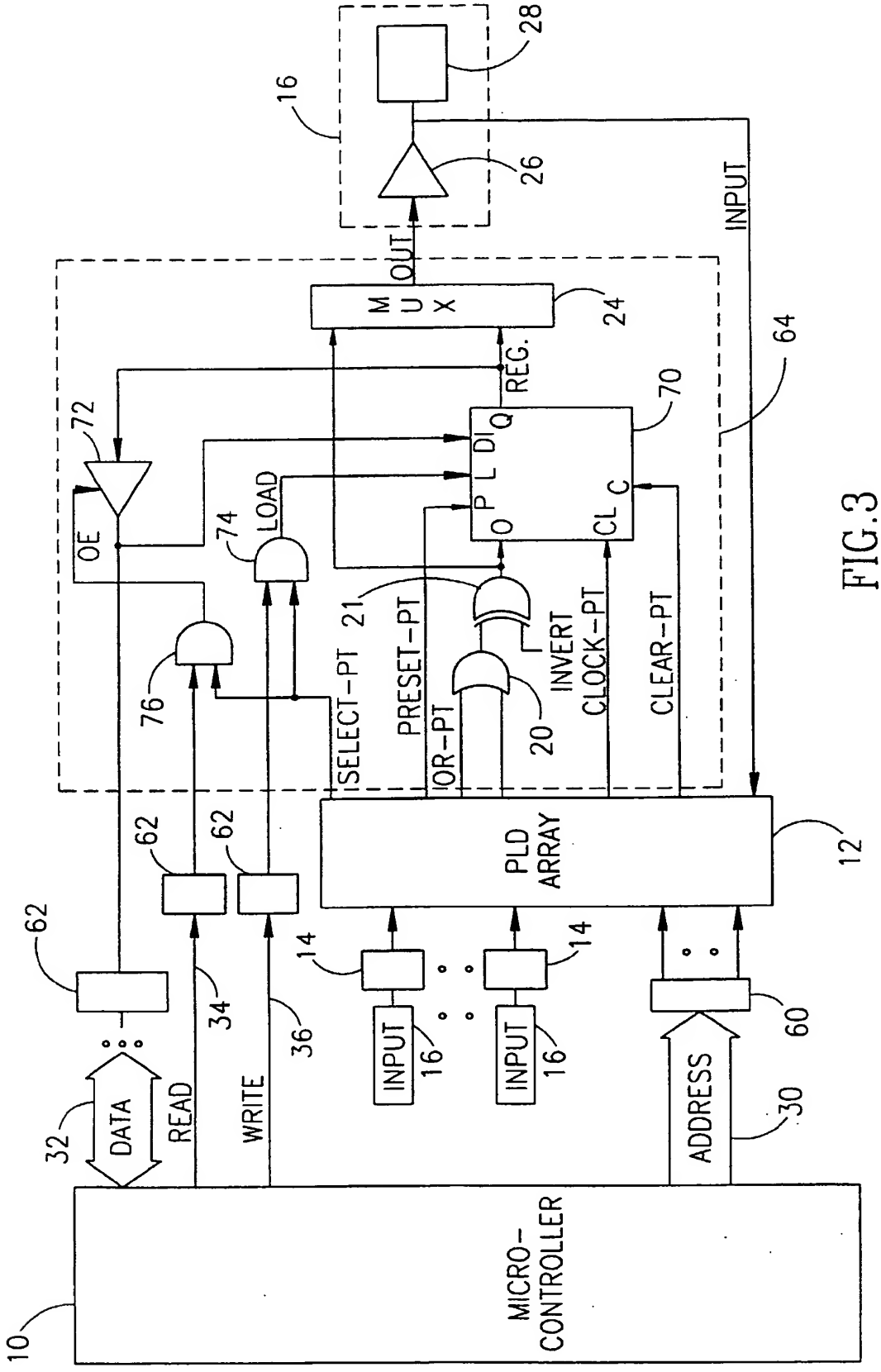
MICRO-CONTROLLER
10
DATA
32
READ
WRITE
34
36
ADDRESS
30
60
INPUT
16
INPUT
16
14
14
PLD ARRAY
12
62
62
62
SELECT-PT
21
PRESET-PT
OR-PT
20
INVERT
CLOCK-PT
CLEAR-PT
76
74
LOAD
OE
72
P L D Q
O
CL C
70
REG.
MUX
24
OUT
16
26
28
INPUT
64

FIG.3

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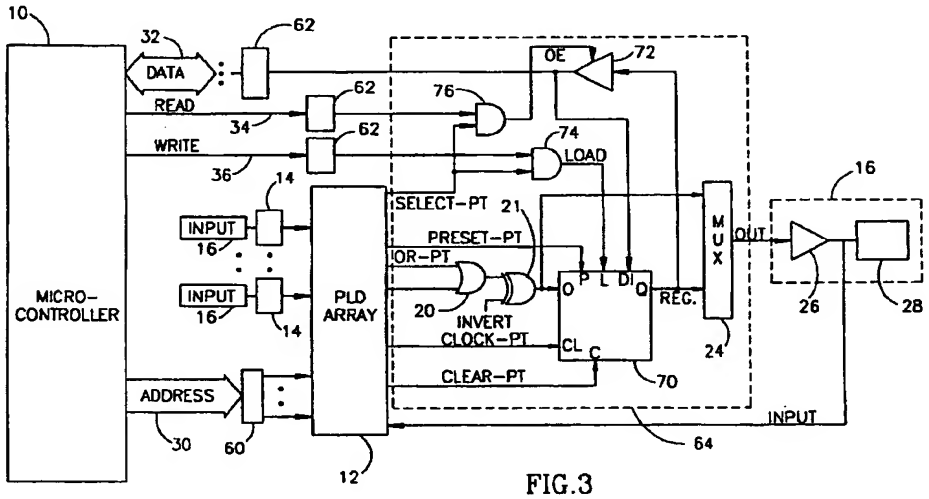

FIG.3

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 97 11 8964

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